

Answers to Student's Book

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10 Boolean logic

Answers to activities

10.1

A	B	A AND NOT B	NOT A AND B	(A AND NOT B) OR (NOT A AND B)	A OR B	NOT (A AND B)	(A OR B) AND (NOT (A AND B))
0	0	0	0	0	0	1	0
0	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1
1	1	0	0	0	1	0	0

10.2

1 a

A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

b

A	B	X
0	0	0
0	1	0
1	0	0
1	1	0

c

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

d

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

e

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

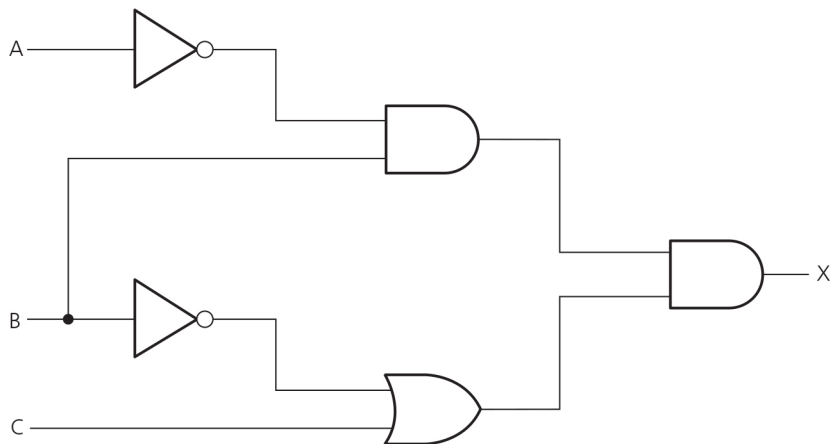
- 2 a** (A AND B) XOR (B NOR C)
b (A NAND C NAND A) NOR (B NOR C)

10.3

1 i

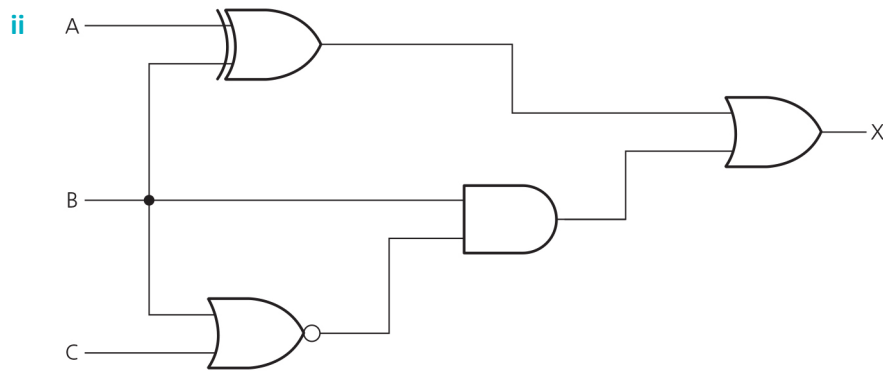
A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

ii



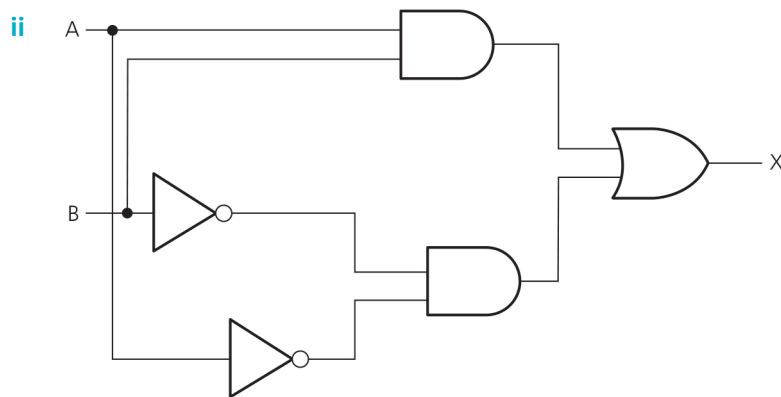
2 i

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0



3 i (NOT A AND NOT B) OR (A AND B)

[or $(\bar{a}.\bar{b}) + (a.b)$]



4 a (NOT A AND NOT B AND NOT C) OR (A AND NOT B AND NOT C) OR (A AND NOT B AND C)

or

$(\bar{a}.\bar{b}.\bar{c}) + (a.\bar{b}.\bar{c}) + (a.\bar{b}.c)$

b (NOT A AND NOT B AND C) OR (NOT A AND B AND NOT C) OR (A AND NOT B AND NOT C) OR (A AND NOT B AND C)

or

$(\bar{a}.\bar{b}.c) + (\bar{a}.b.\bar{c}) + (a.\bar{b}.\bar{c}) + (a.\bar{b}.c)$

- 5 a (NOT A AND NOT B AND NOT C) OR (NOT A AND NOT B AND C) OR (A AND NOT B AND NOT C) OR (A AND NOT B AND C)

or

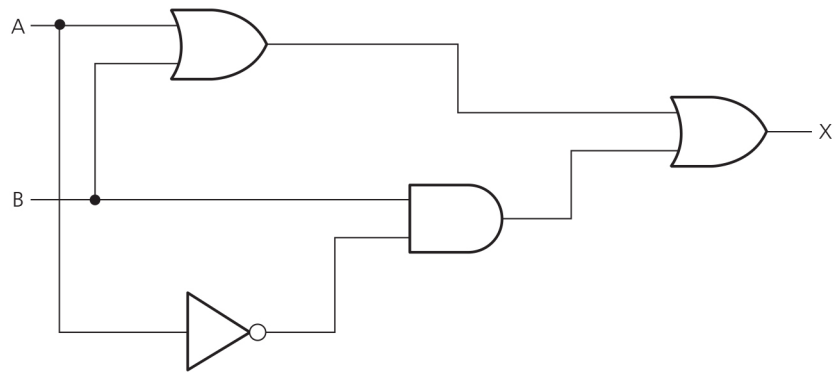
$$(\bar{a}.\bar{b}.\bar{c}) + (\bar{a}.\bar{b}.c) + (a.\bar{b}.\bar{c}) + (a.\bar{b}.c)$$

b

A	B	C	X	NOT A AND NOT B	A AND NOT B	(NOT A AND NOT B) OR (A AND NOT B)
0	0	0	1	1	0	1
0	0	1	1	1	0	1
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	1	0	1	1
1	0	1	1	0	1	1
1	1	0	0	0	0	0
1	1	1	0	0	0	0

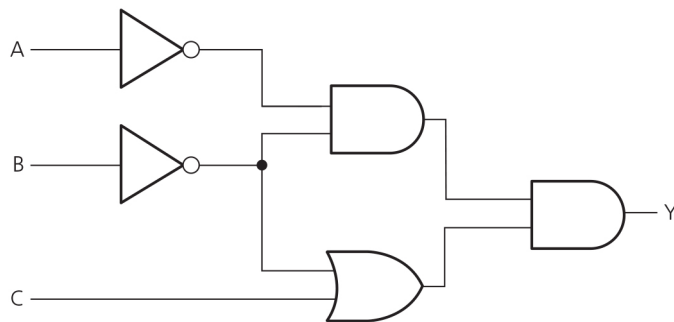
10.4

1 a



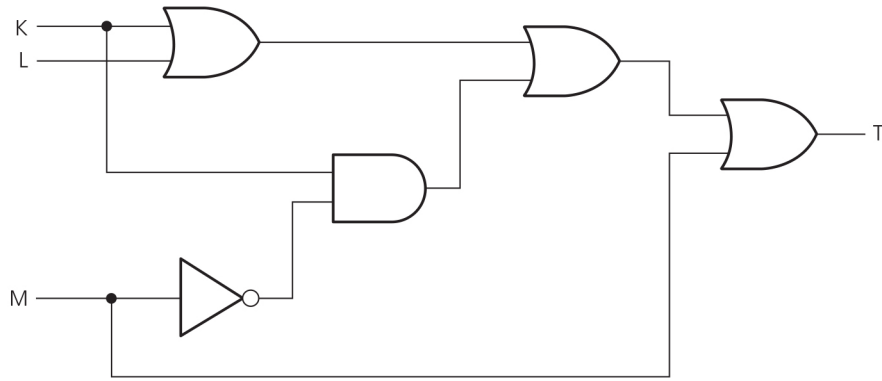
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

b



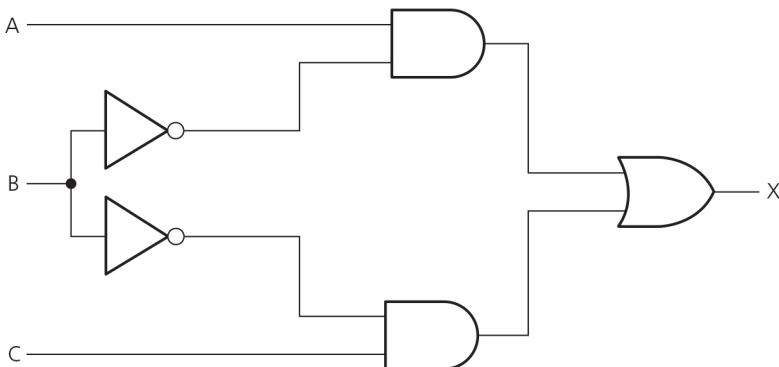
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

c

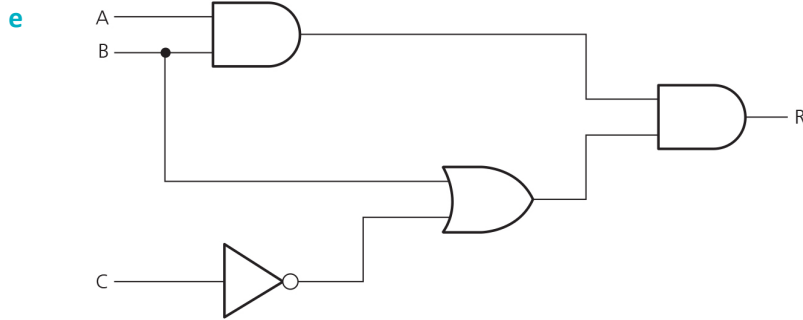


K	L	M	T
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

d



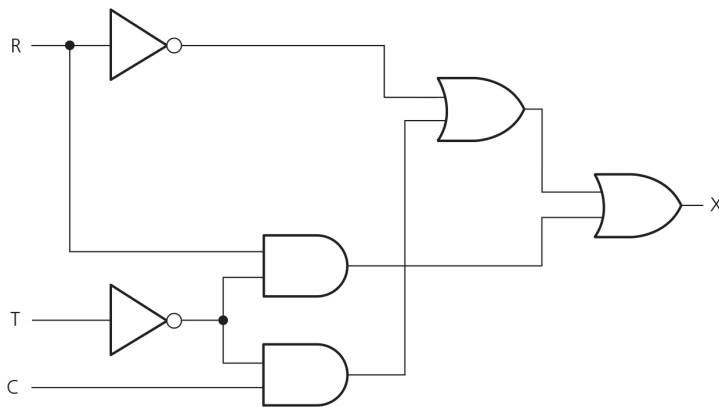
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0



A	B	C	R
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

- 2 Logic statement: (NOT R) OR (C AND NOT T) OR (R AND NOT T)

Logic circuit:

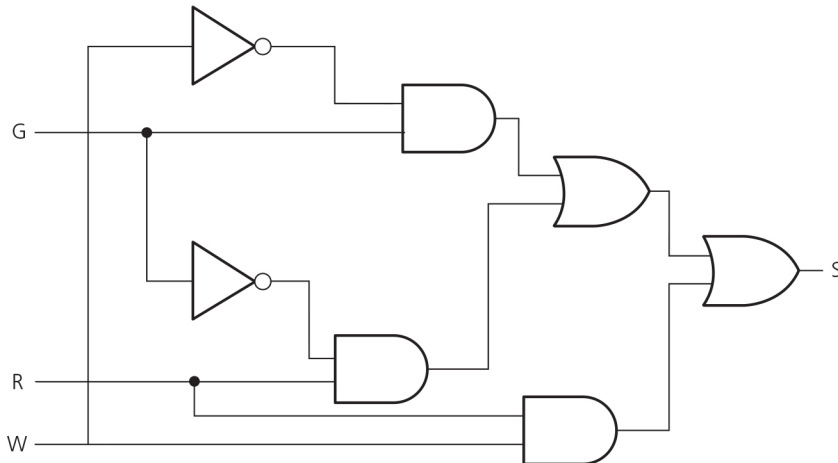


Truth table:

R	T	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

- 3 Logic statement: $(G \text{ AND NOT } W) \text{ OR } (\text{NOT } G \text{ AND } R) \text{ OR } (W \text{ AND } R)$

Logic circuit:



Truth table:

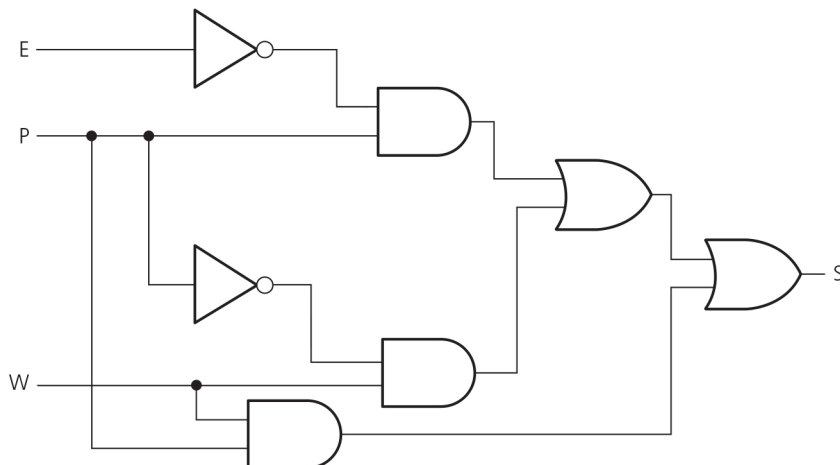
G	R	W	S
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

4 i Truth table:

E	P	W	S
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

ii Logic statement: $(\text{NOT } E \text{ AND } P) \text{ OR } (\text{NOT } P \text{ AND } W) \text{ OR } (P \text{ AND } W)$

iii Logic circuit:



5

A	B	A AND B	NOT A AND NOT B	(A AND B) OR (NOT A AND NOT B)	X
0	0	0	1	1	1
0	1	0	0	0	0
1	0	0	0	0	0
1	1	1	0	1	1

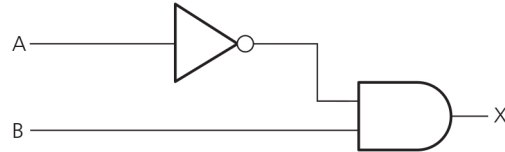
Answers to exam-style questions

Answers to question 5 in this section are example answers for past paper questions. The details of the relevant past paper can be found with the corresponding exam-style question in the Student's Book.

1 a i NOT A AND B

($\bar{a}.b$)

ii



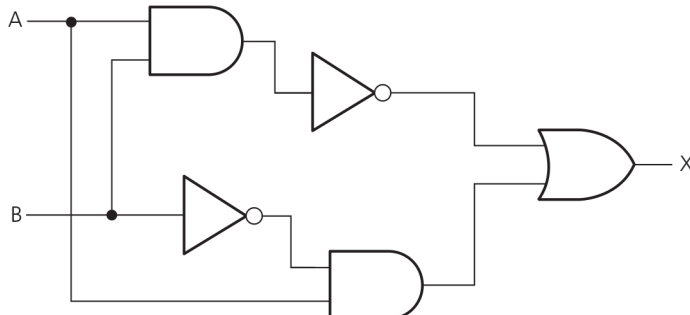
b i (A AND (A NAND B)) NOR (B NOR C)

ii

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

2 a (A AND B) NOR (NOT A AND NOT B)

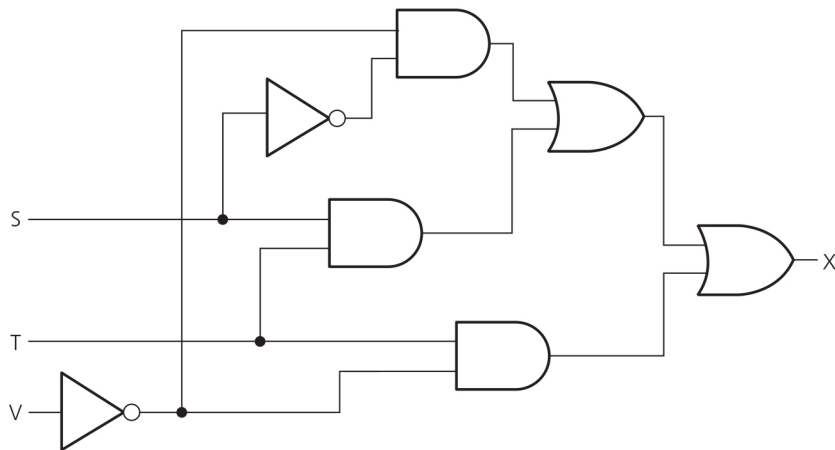
b



c

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

- 3 a** (S AND T) OR (NOT S AND NOT V) OR (T AND NOT V)



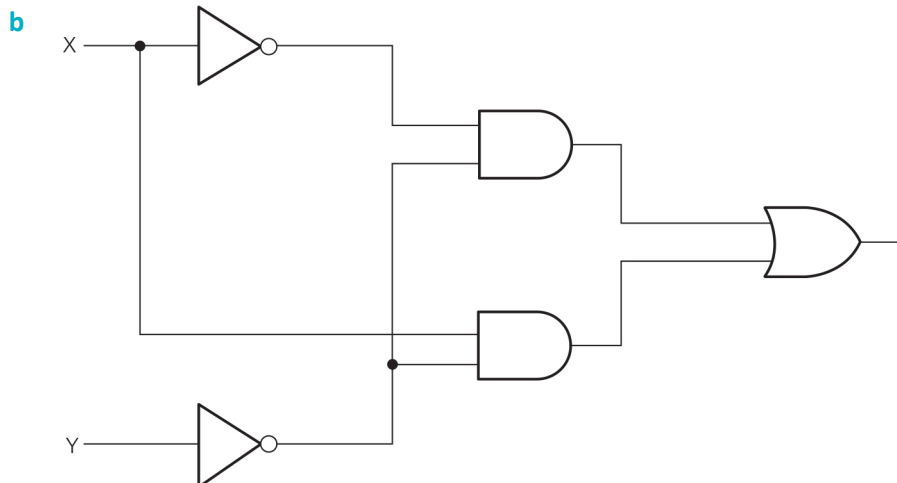
b

S	T	V	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

- 4 a** (NOT X AND NOT Y) OR (X AND NOT Y)

or in alternative notation:

$$\bar{x}.\bar{y} + x.\bar{y}$$

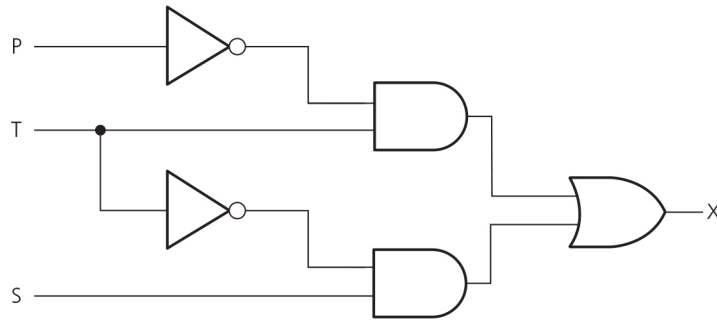


5 a

A	B	OUTPUT
0	0	0
0	1	1
1	0	1
1	1	1

b XOR gate

c (T AND NOT P) OR (S AND NOT T)

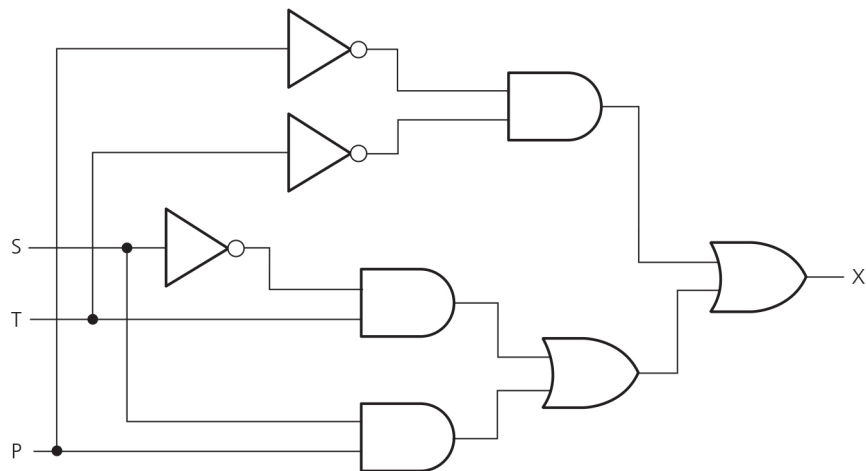


d Two from:

- continuous measurements taken
- won't forget to take readings
- more accurate readings
- safer since no human in contact with potentially dangerous process
- cost saving since no need to pay any wages

6 a (NOT S AND T) OR (S AND P) OR (NOT T AND NOT P)

b



c

S	T	P	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Chapter 10 Extension Answers

Task 1

A	B	F	X
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

This truth table is the same as an AND gate.

A	B	F	G	X
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

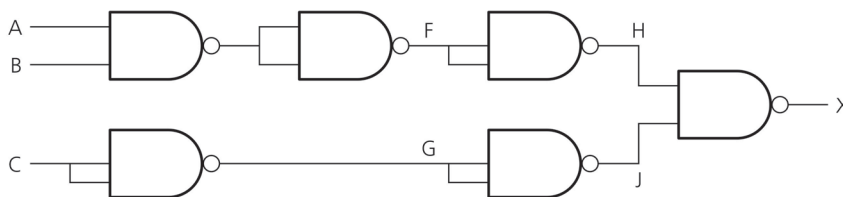
This truth table is the same as an OR gate.

A	F	X
0	0	1
1	1	0

This truth table is the same as a NOT gate.

Task 2

- 1 We simply replace each AND, OR and NOT gate with the NAND gate equivalents given in Figure 10.34:



To confirm we can write down both truth tables. First, for the circuit shown in the question:

A	B	C	J	K	X
0	0	0	0	1	1
0	0	1	0	0	0
0	1	0	0	1	1
0	1	1	0	0	0
1	0	0	0	1	1
1	0	1	0	0	0
1	1	0	1	1	1
1	1	1	1	0	1

Then, for the equivalent NAND circuit we have drawn:

A	B	C	F	G	H	J	X
0	0	0	0	1	1	0	1
0	0	1	0	0	1	1	0
0	1	0	0	1	1	0	1
0	1	1	0	0	1	1	0
1	0	0	0	1	1	0	1
1	0	1	0	0	1	1	0
1	1	0	1	1	0	0	1
1	1	1	1	0	0	1	1

The yellow highlights show the inputs and outputs for both circuits, which are the same, and therefore the circuits are equivalent.

- 2 One way to approach this is to first consider the XOR truth table, which is what we want to achieve:

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

We can see how close this is to an OR gate truth table:

A	B	F	G	X
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

The only row we need to amend from the OR gate truth table is the final one. We require F and G to both be 1 so that $X = F \text{ NAND } G$ is 0 on that final row, i.e.:

A	B	F	G	X
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	1	1	0

It is only when A and B are both 1 that we want to amend the OR gate circuit. A NAND could be used to do this, because a NAND gate has the property that only when both inputs are 1 is the output different:

A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

How can we combine A NAND B with A in order that F has the values we require?

By combining gates as follows:

A	B	A NAND B	F
0	0	1	1
0	1	1	1
1	0	1	0
1	1	0	0

It can be seen that $F = A \text{ NAND } (A \text{ NAND } B)$.

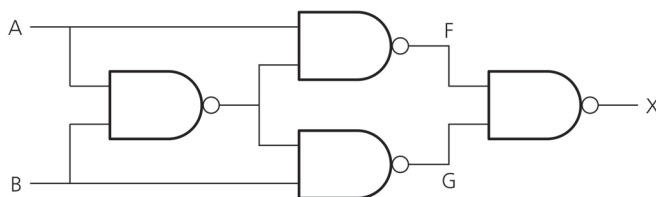
We can use the same approach for G, but this time considering the input B:

A	B	A NAND B	$F = A \text{ NAND } (A \text{ NAND } B)$	$G = B \text{ NAND } (A \text{ NAND } B)$
0	0	1	1	1
0	1	1	1	0
1	0	1	0	1
1	1	0	1	1

We now have the values of F and G that will ensure the output X (which is still $X = F \text{ NAND } G$ as per the OR circuit) behaves like an XOR gate:

A	B	$F = A \text{ NAND } (A \text{ NAND } B)$	$G = B \text{ NAND } (A \text{ NAND } B)$	X
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	1	1	0

Let's draw the circuit:



Task 3

A	B	F	G	H	X
0	0	1	1	0	1
0	1	1	0	1	0
1	0	0	1	1	0
1	1	0	0	1	0

By considering only the inputs A, B and the output X we can see this is the inverse of an OR gate, which is called an **NOR gate**.